USB5936
User’s Manual

Beijing ART Technology Development Co., Ltd.

Contents

Chapter 1 Overview

USB5936 data acquisition board is compatible with USB bus, may access the computer via USB cable, which constitutes the laboratory, product quality testing center, field monitoring and control, medical equipment and other fields' data acquisition, waveform analysis and processing system, it can also constitute the industrial production process control monitoring system. And it has a small size, plug-and-play characteristics, so it is the best choice for portable system.

Unpacking Checklist

Check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the local dealer or sales for a replacement. Retain the shipping carton and packing material for inspection by the dealer.
Check for the following items in the package. If there are any missing items, contact your local dealer or sales.

- USB5936 Data Acquisition Board
- ART Disk
  a) user's manual (pdf)
  b) drive
  c) catalog
- Warranty Card

FEATURES

Analog Input

- Converter Type: AD7321
- Input Range: ±10V, ±5V, ±2.5, 0~10V
- 12-bit resolution, the13 bit is the sign bit
- Sample Frequency: 1Hz~250KHz
  Frequency Formula: sampling frequency= main frequency/the number of frequency division, main frequency = 10MHz, 32-bit frequency division, the number of frequency division range: 40~10^7.
- Number of Channels: 16SE/8DI
- Data Read Mode: non-empty and half-full
- Memory Depth: 16K word FIFO memory
- Memory Signs: non-empty and half-full
- AD Mode: continuum sampling , grouping sampling
- Group Interval: software-configurable, minimum value is sampling period, maximum value is 419430μs
- Loops of Group: software-configurable, minimum value is one time , maximum value is 255 times
- Clock Source: internal clock
- Analog Input Impedance: 10 MΩ
- Programmable amplifier type: AD8251(default), compatible AD8250, AD8253
- Programmable Gain: 1, 2, 4, 8 (AD8251 default) or 1, 2, 5, 10 (AD8250) or 1, 10, 100, 1000 (AD8253)
- Amplifier Set-up Time: 785ns(0.001%)(max)
- Non-linear error: ±1LSB(Maximum)
- System Measurement Accuracy: 0.1%
- Operating Temperature Range: 0℃~50℃
- Storage Temperature Range: −20℃~70℃

Digital Input

- Channel No.: 6-channel
- Electric Standard: TTL compatible
- Maximum Sink Current: <0.5V
- High Level: ≧2V
- Low Level: ≦0.8V

Digital Output

- Channel No.: 6-channel
- Electrical Standard: CMOS compatible
- High Level: ≧4.45V
- Low Level: ≦0.5V
- Power-on Output: low level

CNT Counter/timer

- one 24-bit counter/timer
- Count Mode: six counting modes (software configurable)
- Input and Output Electrical Standard: TTL level
- Clock Source (CLK): the frequency range is 1Hz ~ 10MHz
- Gate (GATE): rising edge, high level, low level
- Counter Output (OUT): high level, low level

Other Features

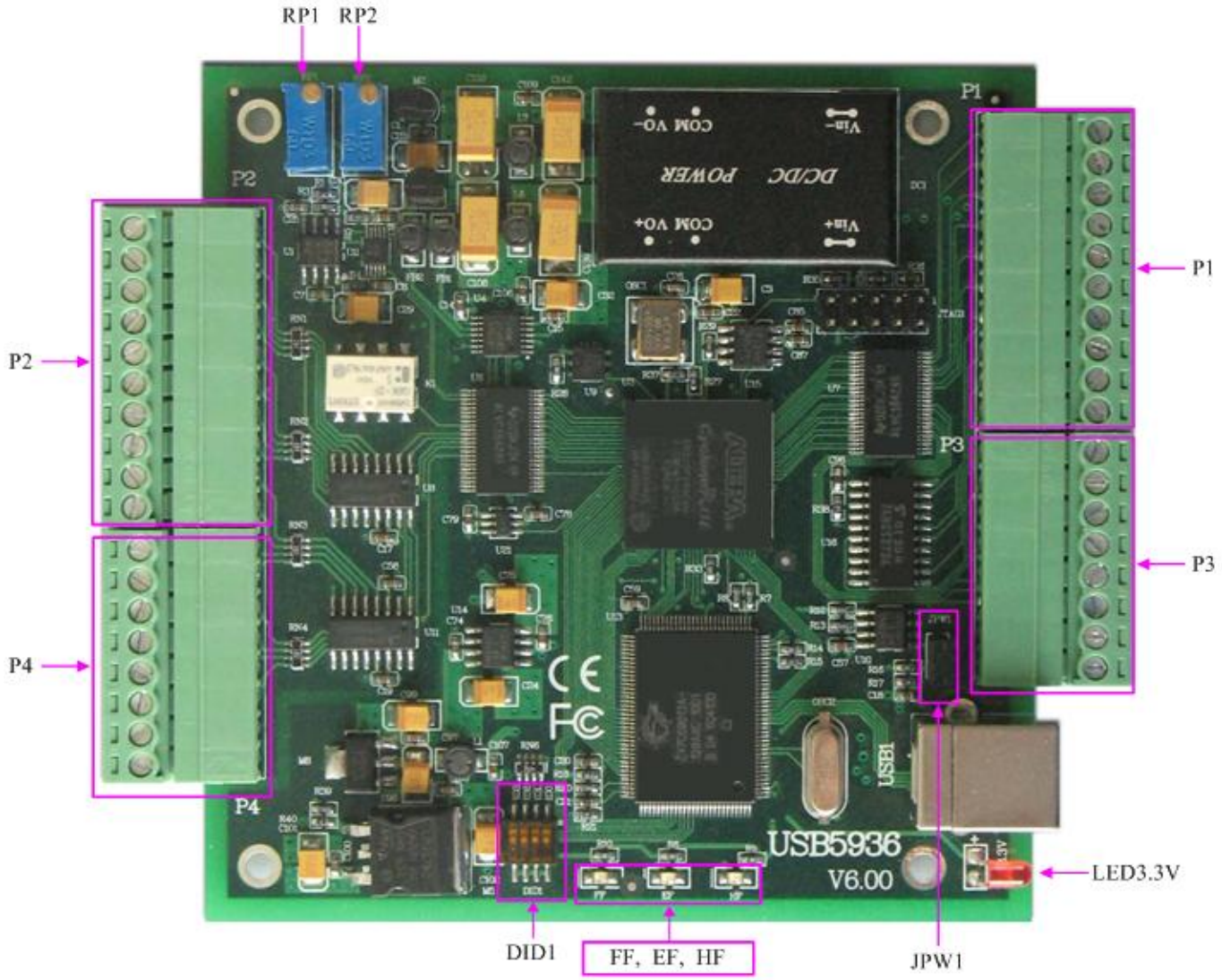
Board Clock Oscillation: 10MHz

Board Dimension: 95.7mm (L) * 98.84mm (W) * 15.7mm (H)

Case Dimension: 99mm (L) * 107.7mm (W) * 26.3mm (H)

Chapter 2 Components Layout Diagram and a Brief Description

2.1 The Main Components Layout Diagram



2.2 The Function Description for the Main Component

2.2.1 Signal Input and Output Connectors

P2, P4: analog signal input connectors

P1, P3: digital signal input/output and counter input/output connectors

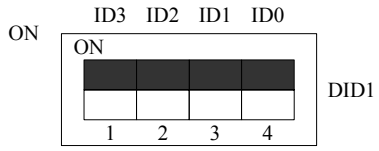
2.2.2 Potentiometer

RP1: Analog signal input zero-point adjustment potentiometer

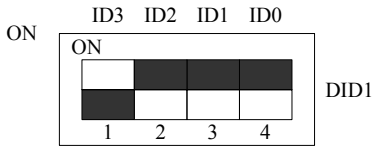
RP2: Analog signal input full-scale adjustment potentiometer

2.2.3 Physical ID of DIP Switch

DID1: Set physical ID number. When the PC is installed more than one USB5936 , you can use the DIP switch to set a physical ID number for each board, which makes it very convenient for users to distinguish and visit each board in the progress of the hardware configuration and software programming. The following four-place numbers are expressed by the binary system: When DIP switch points to "ON", that means "1", and when it points to the other side, that means "0." As they are shown in the following diagrams: place "ID3" is the high place."ID0" is the low place, and the black part in the diagram represents the location of the switch. (Test softwares of the company often use the logic ID management equipments and at this moment the physical ID DIP switch is invalid. If you want to use more than one kind of the equipments in one and the same system at the same time, please use the physical ID as much as possible).



The above chart shows"1111", so it means that the physical ID is 15.



The above chart shows"0111", so it means that the physical ID is 7.

The above chart shows"0101", so it means that the physical ID is 5.

ID3	ID2	ID1	ID0	物理ID（Hex）	物理ID（Dec）
OFF（0）	OFF（0）	OFF（0）	OFF（0）	0	0
OFF（0）	OFF（0）	OFF（0）	ON（1）	1	1
OFF（0）	OFF（0）	ON（1）	OFF（0）	2	2
OFF（0）	OFF（0）	ON（1）	ON（1）	3	3
OFF（0）	ON（1）	OFF（0）	OFF（0）	4	4
OFF（0）	ON（1）	OFF（0）	ON（1）	5	5
OFF（0）	ON（1）	ON（1）	OFF（0）	6	6
OFF（0）	ON（1）	ON（1）	ON（1）	7	7
ON（1）	OFF（0）	OFF（0）	OFF（0）	8	8
ON（1）	OFF（0）	OFF（0）	ON（1）	9	9
ON（1）	OFF（0）	ON（1）	OFF（0）	A	10
ON（1）	OFF（0）	ON（1）	ON（1）	B	11
ON（1）	ON（1）	OFF（0）	OFF（0）	C	12
ON（1）	ON（1）	OFF（0）	ON（1）	D	13

ON（1）	ON（1）	ON（1）	OFF（0）	E	14
ON（1）	ON（1）	ON（1）	ON（1）	F	15

2.2.4 Status Indicator

LED3.3V: 3.3V power indicator, on for normal condition.

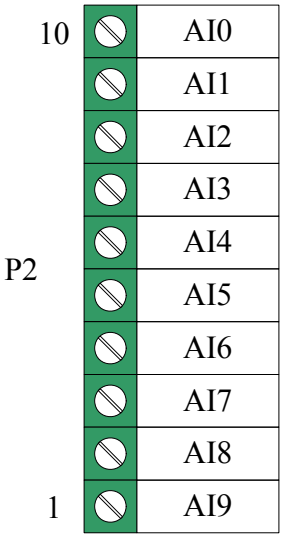
2.2.5 Jumper

JPW1: load the USB controller program, and 1-2 pin shorted (default).

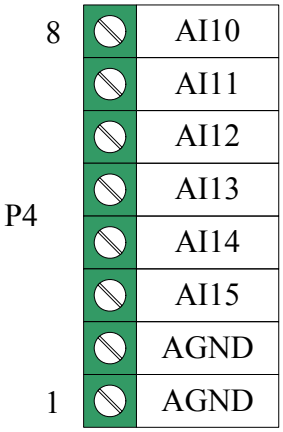
Chapter 3 Signal Connectors

3.1 The Definition of Signal Input Connectors

Pin definition of P2



Pin definition of P4

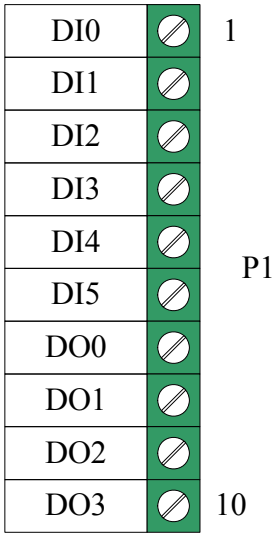


Pin definition about analog inputs

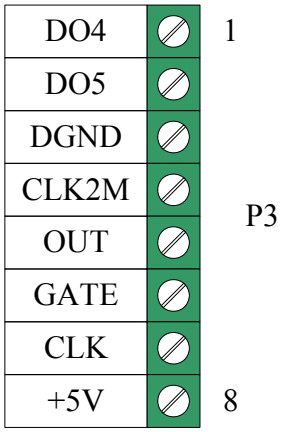
Pin name	Pin feature	Pin function definition
AI0-AI15	Input	Analog input pins
AGAN	GND	Analog signals ground

3.2 The Definition of Digital Signal Connectors

Pin definition of P1



Pin definition of P3



Pin definition

Pin name	Type	Pin function definition
DI0~DI5	Input	Digital input, reference ground is DGND.
DO0～DO5	Output	Digital output.
+5V	Output	Output 5V voltage.
CLK2M	Output	On-board 2.5MHz clock oscillator pulse output, output cycle 0.4 microseconds, provides the clock source signal for CLK
CLK	Input	Timer/counter clock source input, reference ground is DGND. When use external clock as counter clock, the clock frequency not exceeding 20MHz. The default counter clock is internal clock LOCAL_CLK, frequency range: 620Hz~20MHz.
GATE	Input	Timer/counter gate input, reference ground is DGND.
OUT	Output	Timer/Counter output, only clock output is forbidden, it is counter output, if it is not forbidden, it is AD clock output CLKOUT. The default is counter output, reference ground is DGND.
DGND		Digital ground. Ground reference for Digital circuitry. This DGND pin should be connected to the system's DGND plane.

Chapter 4 Connection Ways for Each Signal

4.1 Analog Input Connection Mode

4.1.1 Single-ended Input Connection Mode

Single-ended mode can achieve a signal input by one channel, and several signals use the common reference ground. This mode is widely applied in occasions of the small interference and relatively many channels.

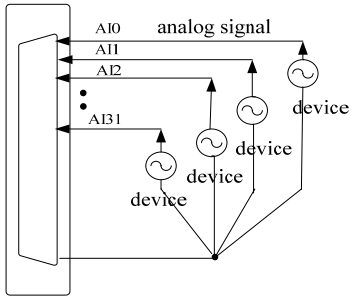


Figure 4.1.1 single-ended input connection

4.1.2 Differential Input Connection Mode

Differential input mode uses positive and negative channels to input a signal. This mode is mostly used when biggish interference happens and the channel numbers are few. Single-ended/double-ended mode can be set by the software, please refer to USB5936 software manual.

According to the diagram below, USB5936 board can be connected as analog voltage double-ended input mode, which can effectively suppress common-mode interference signal to improve the accuracy of acquisition. Positive side of the 16-channel analog input signal is connected to AI0~AI7, the negative side of the analog input signal is connected to AI8~AI15, equipments in industrial sites share the AGND with USB5936 board.

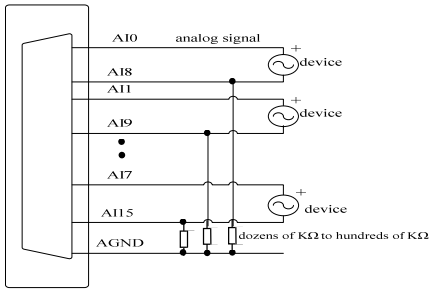
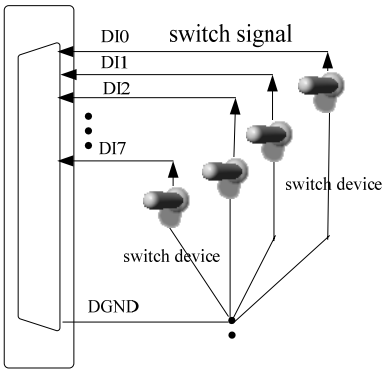
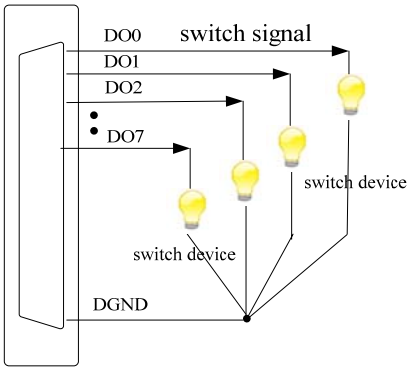


Figure 4.1.2 double-ended input connection

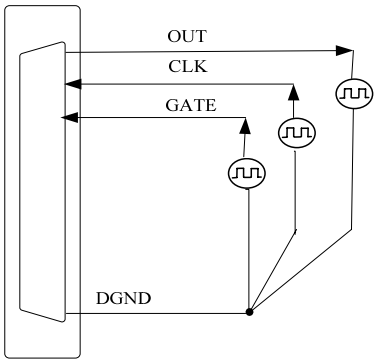
4.2 Digital Input Connection



4.3 Digital Output Connection



4.4 Counter/Timer Connection



Chapter 5 Timer/Counter Function

5.1 The working mode

MODE 0 Interrupt on terminal count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.

GATE=1 enables counting; GATE=0 disables counting. GATE has no effect on OUT.

After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N+1 CLK pulses after the initial count is written.

If a new count is written to the Counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:
1) Writing the first byte disables counting. OUT is set low immediately (no clock pulse required)
2) Writing the second byte allows the new count to be loaded on the next CLK pulse

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N+1 CLK pulses after the new count of N is written.

If an initial count is written while GATE=0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulse later, no CLK pulse is needed to load the Counter as this has already been done.

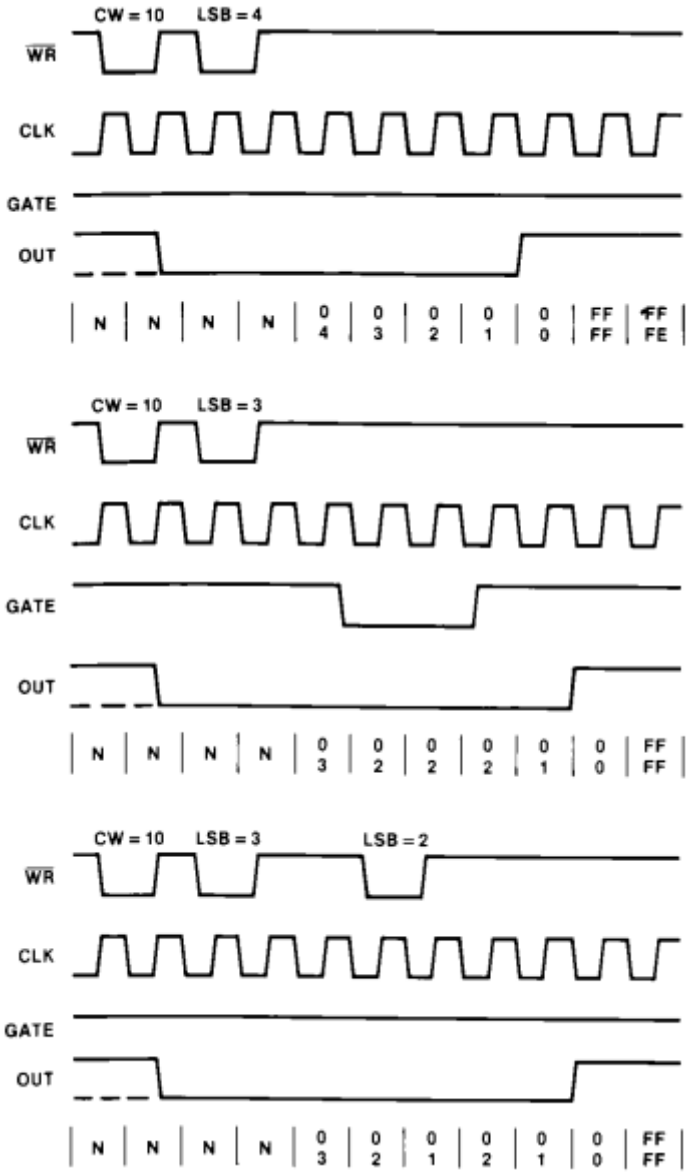


Figure 5.1 Mode 0

NOTE

The following conventions apply to all mode timing diagrams

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.

2. The counter is always selected ($\overline{CS}$ always low)

3. CW stands for "Control Word"; CW=10 means a control word of 10 HEX is written to the counter.

4. LSB stands for "Least Significant Byte" of count.

5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte.

Since the counter is programmed to read/writer LSB only, the most significant byte cannot be read.

N stands for an undefined count.

Vertical lines show transitions between count values.

MODE 1 Hardware retriggerable one-shot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero.

OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse. An initial count of N will result in a one-shot pulse N CLK cycles in duration. The one-shout is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

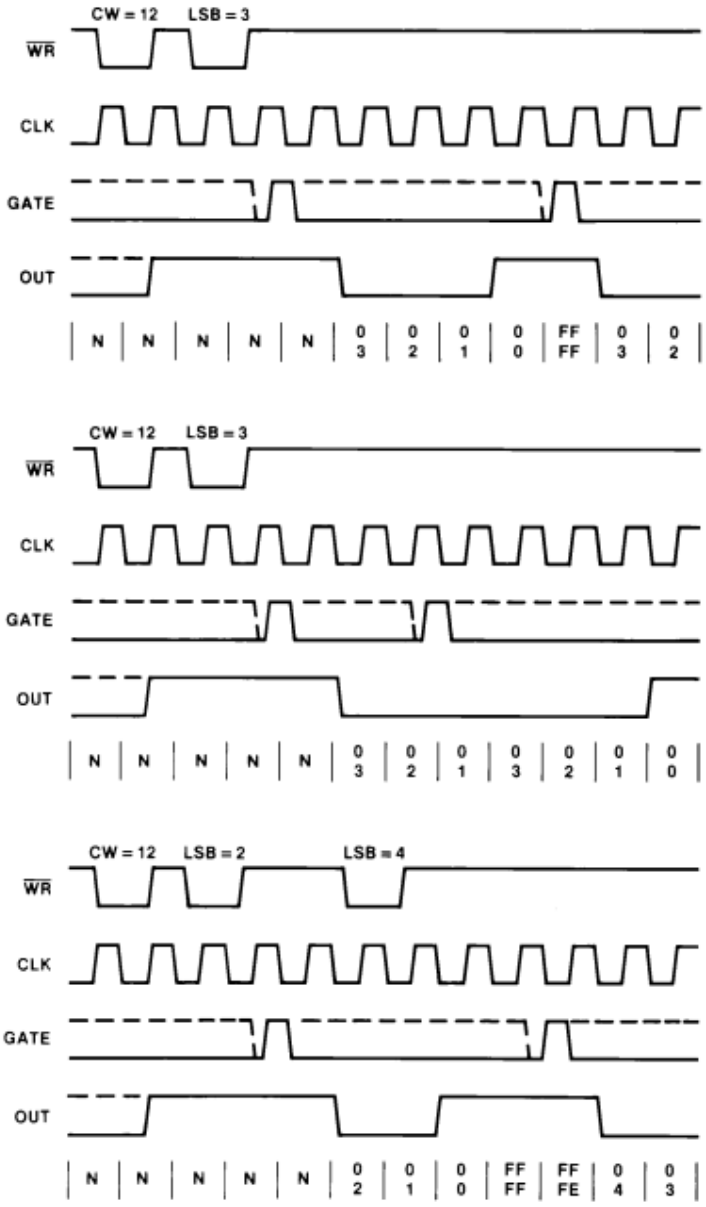


Figure 5.2 Mode 1

MODE 2 Rate Generator

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for on CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE=1 enables counting; GATE=0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.
After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK Pulses after the initial count is written. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle. In mode2, a COUNT of 1 I illegal.

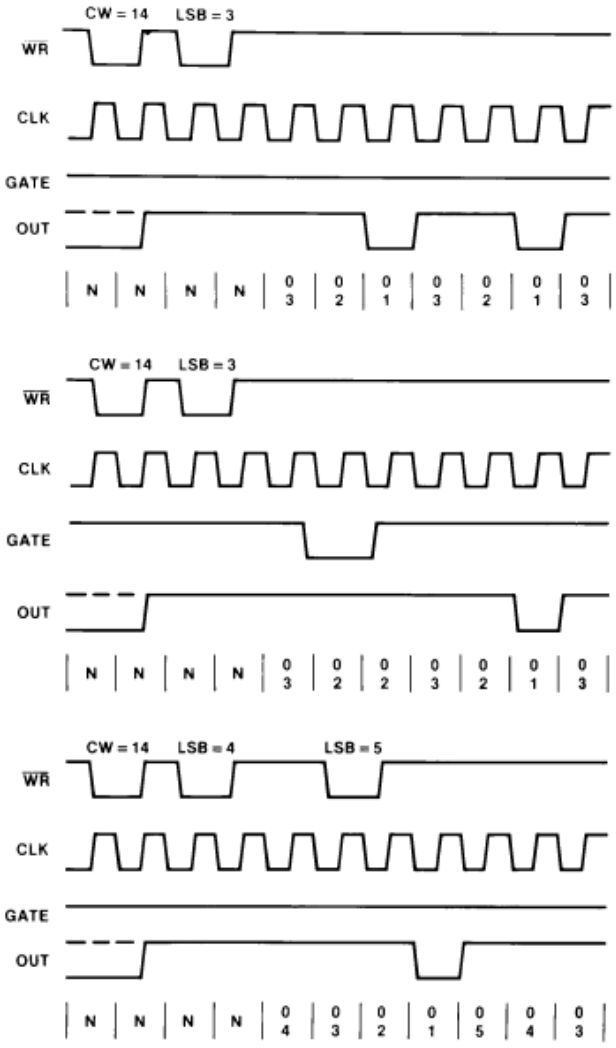


Figure 5.3 Mode 2

Note: A GATE transition should not occur one clock prior to terminal count.

MODE 3 Square wave mode

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for mainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE=1 enables counting; GATE=0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new counter will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.
Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse after the count expires. OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts, OUT will be high for (N+1)/2 counts and low for (N-1)/2 counts.

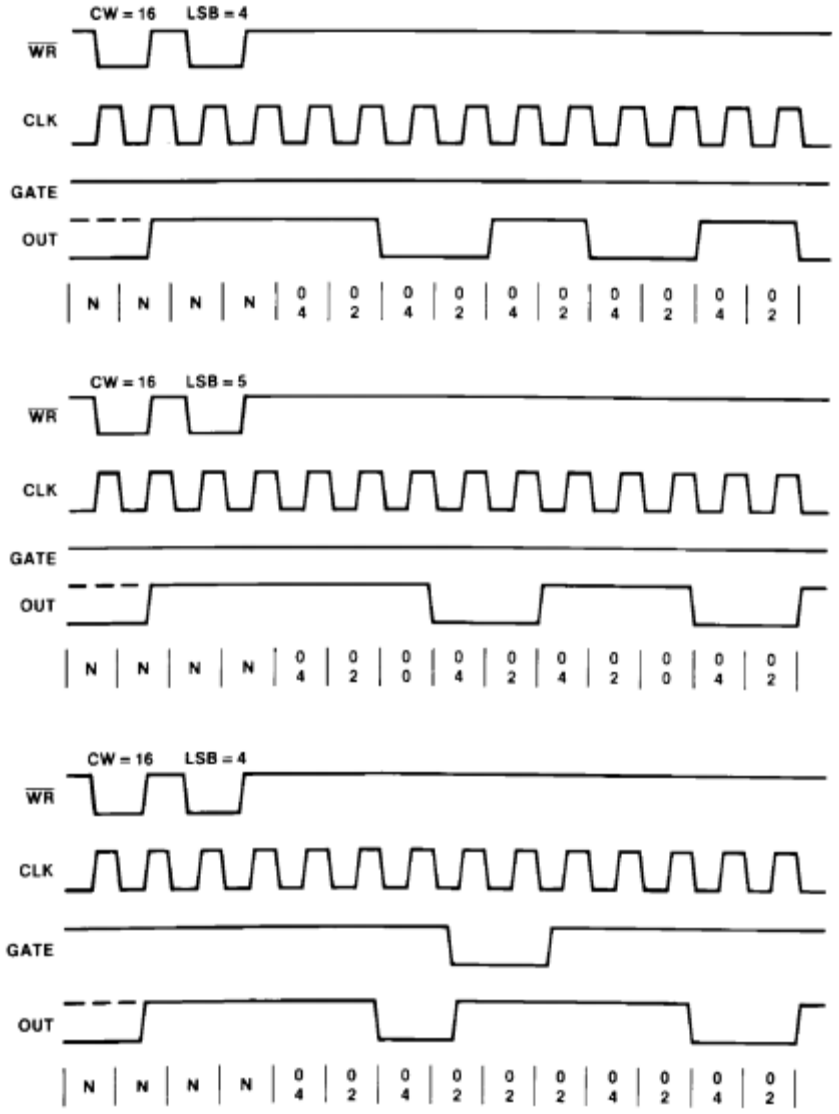


Figure 5.4 Mode 3

Note: A GATE transition should not occur one clock prior to terminal count.

MODE 4 Software triggered strobe

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is “triggered” by writing the initial count.

GATE=1 enables counting; GATE=0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N+1 CLK pulses after the initial count is written.

If a new count is written during counting, if will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte has no effect on counting.

2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be ‘‘retriggered’ by software. OUT strobe low N+1 CLK pulses after the new count of N is written.

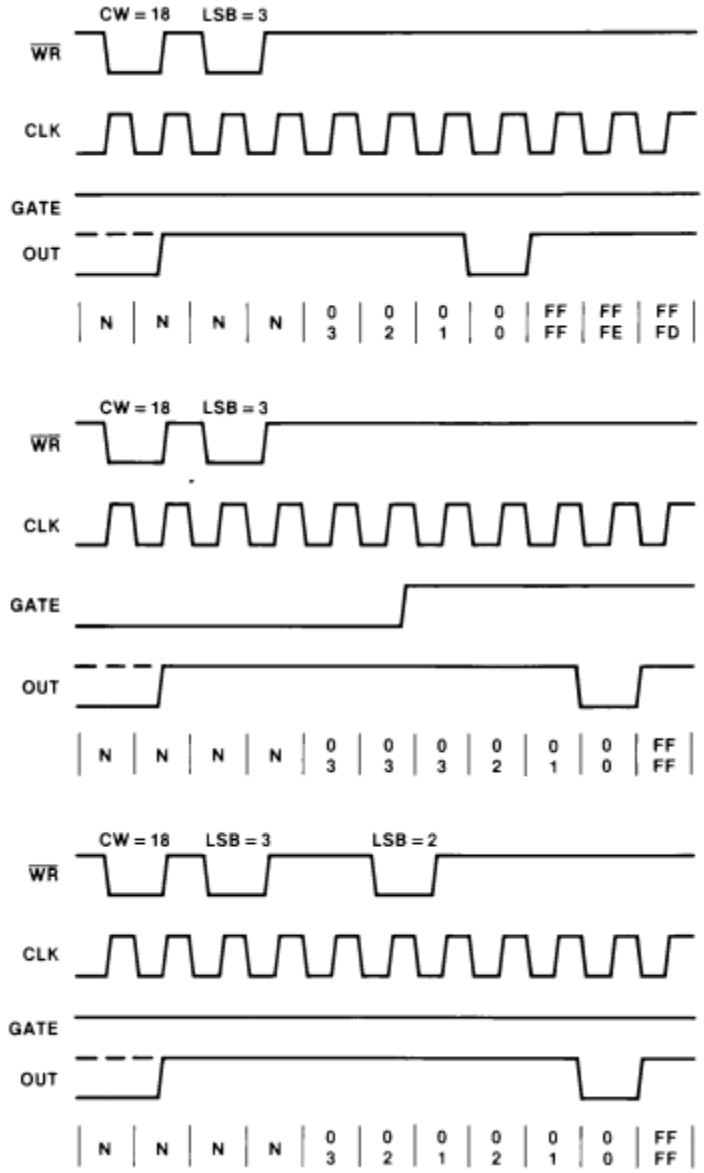


Figure 5.5 Mode 4

MODE 5 Hardware triggered strobe

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N+ 1 pulse after a trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for N+1 CLK pulses after any trigger. GATE has no effect on OUT.
If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

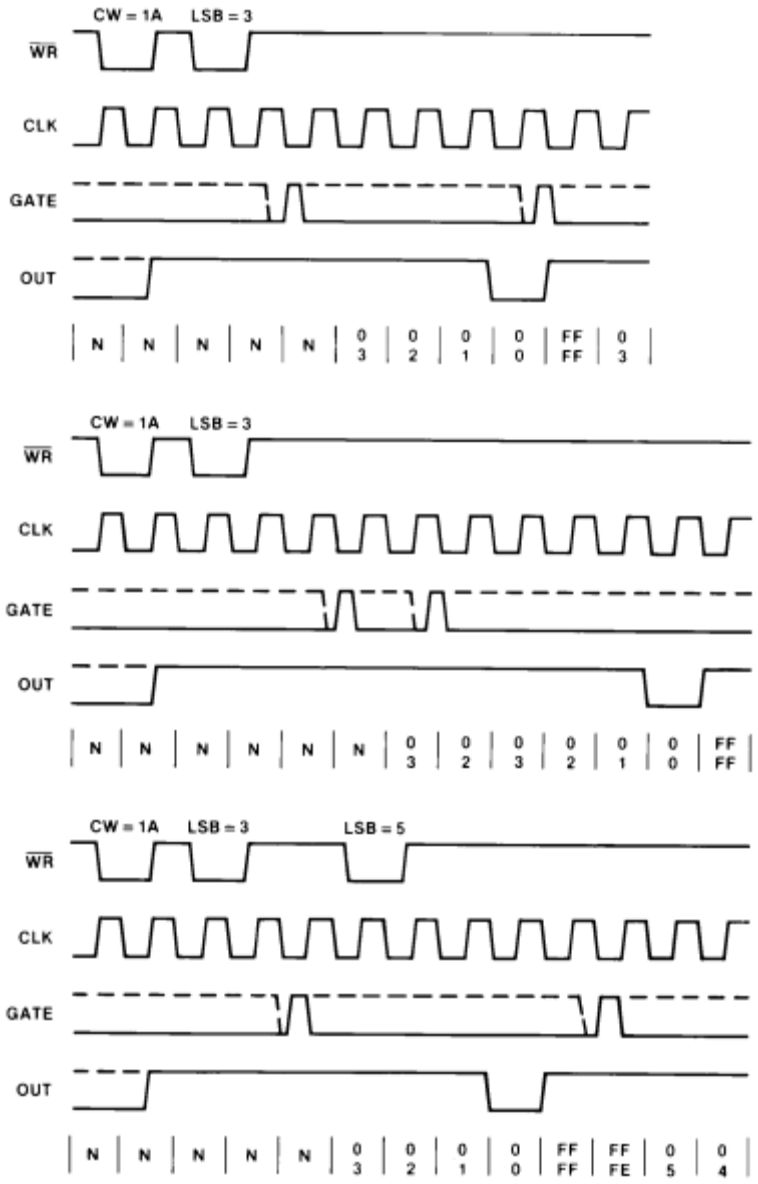


Figure 5.6 Mode 5

Chapter 6 Notes, Calibration and Warranty Policy

6.1 Notes

In our products' packing, user can find a user manual, a USB5936 module and a quality guarantee card. Users must keep quality guarantee card carefully, if the products have some problems and need repairing, please send products together with quality guarantee card to ART, we will provide good after-sale service and solve the problem as quickly as we can.

When using USB5936, in order to prevent the IC (chip) from electrostatic harm, please do not touch IC (chip) in the front panel of USB5936 module.

6.2 Analog Input Calibration

Every device has to be calibrated before sending from the factory. It is necessary to calibrate the module again if users want to after using for a period of time or changing the input range. USB5936 default input range: ±10V, in the manual, we introduce how to calibrate USB5936 in ±10V, calibrations of other input ranges are similar.

Prepare a digital voltage instrument which the resolution is more than 5.5 bit, install the USB5936 module, and then power on, warm-up for fifteen minutes.

1) Zero adjustment: select one channel of analog inputs, take the channel AI0for example, connect 0V to AI0, other channels connect with the ground, and then run ART Data Acquisition Measurement Suite in the WINDOWS. Choose channel 0, ±10V input range and start sampling, adjust potentiometer RP1 in order to make voltage value is 0.000V or about 0.000V. Zero adjustment of other channels is alike.
2) Full-scale adjustment: select one channel of analog inputs, take the channel AI1 for example, connect 9997.55mV to AI1, other channels connect with the ground, and then run ART Data Acquisition Measurement Suite in the WINDOWS. Choose channel 0, ±10V input range and start sampling, adjust potentiometer RP2 in order to make voltage value is 9997.55mV or about 9997.55mV. Full-scale adjustment of other channels is alike.
3) Repeat steps above until meet the requirement.

6.3 Warranty Policy

Thank you for choosing ART. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ART's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: www.art-control.com.

2. All ART products come with a limited two-year warranty:

- The warranty period starts on the day the product is shipped from ART's factory
- For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ART is not responsible for any loss of data.
- Please ensure the use of properly licensed software with our systems. ART does not condone the use of pirated software and will not service systems using such software. ART will not be held legally responsible for products shipped with unlicensed software installed by the user.

3. Our repair service is not covered by ART's guarantee in the following situations:
- Damage caused by not following instructions in the User's Manual.
- Damage caused by carelessness on the user's part during product transportation.
- Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).
- Damage from improper repair by unauthorized ART technicians.
- Products with altered and/or damaged serial numbers are not entitled to our service.

4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.
5. To ensure the speed and quality of product repair, please download an RMA application form from our company website.

Products Rapid Installation and Self-check

Rapid Installation

Product-driven procedure is the operating system adaptive installation mode. After inserting the disc, you can select the appropriate board type on the pop-up interface, click the button【driver installation】or select CD-ROM drive in Resource Explorer, locate the product catalog and enter into the APP folder, and implement Setup.exe file. After the installation, pop-up CD-ROM, shut off your computer, insert the PCI card. If it is a USB product, it can be directly inserted into the device. When the system prompts that it finds a new hardware, you do not specify a drive path, the operating system can automatically look up it from the system directory, and then you can complete the installation.

Self-check

At this moment, there should be installation information of the installed device in the Device Manager (when the device does not work, you can check this item.). Open "Start -> Programs -> ART Demonstration Monitoring and Control System -> Corresponding Board -> Advanced Testing Presentation System", the program is a standard testing procedure. Based on the specification of Pin definition, connect the signal acquisition data and test whether AD is normal or not. Connect the input pins to the corresponding output pins and use the testing procedure to test whether the switch is normal or not.

Delete Wrong Installation

When you select the wrong drive, or viruses lead to driver error, you can carry out the following operations: In Resource Explorer, open CD-ROM drive, run Others-> SUPPORT-> PCI.bat procedures, and delete the hardware information that relevant to our boards, and then carry out the process of section I all over again, we can complete the new installation.